SysML-Companion: Virtual prototyping from SysML models

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Better technical solutions for complex systems

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How to...

- have a common repository for both manager and engineers?
- do early testing of project feasibility and check hypotheses soundness?
- verify functional and non-functional properties on the model?
- easily explore design space?
- test the conformance of final product?
- ease the maintainability of the system?

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Virtual prototyping from SysML

- Write a unique specification in SysML, the *lingua franca* of system engineers
- Do virtual-prototyping from it
- Derive tests from the specification
- Test and optimize with hardware-in-the-loop

RTaW SysML-Companion automatically generates from SysML specification simulable and formally analysable models.

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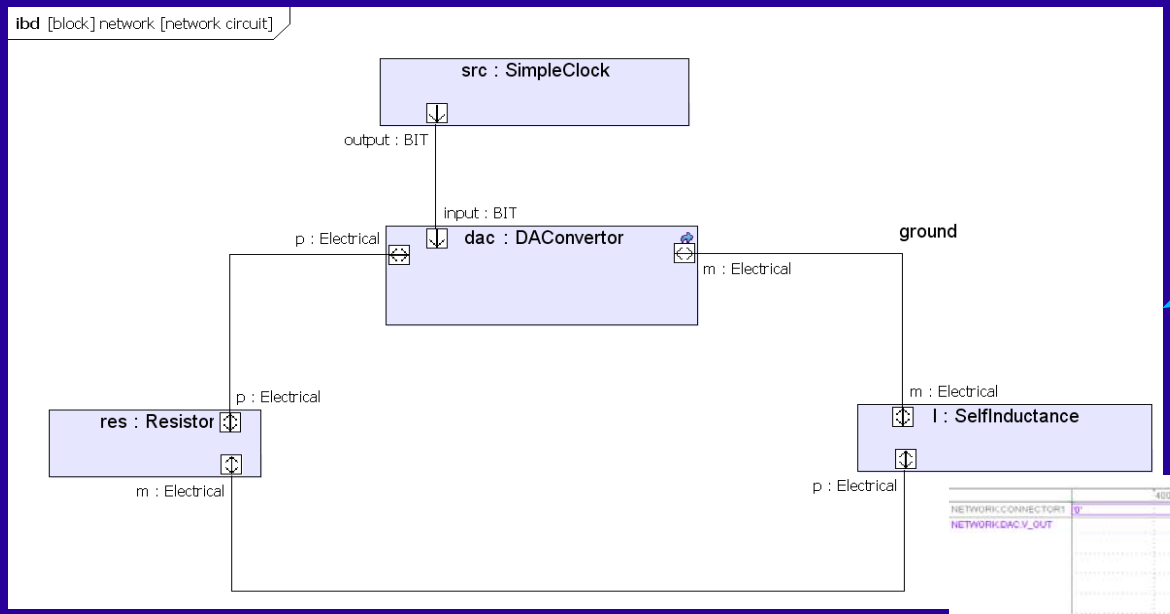
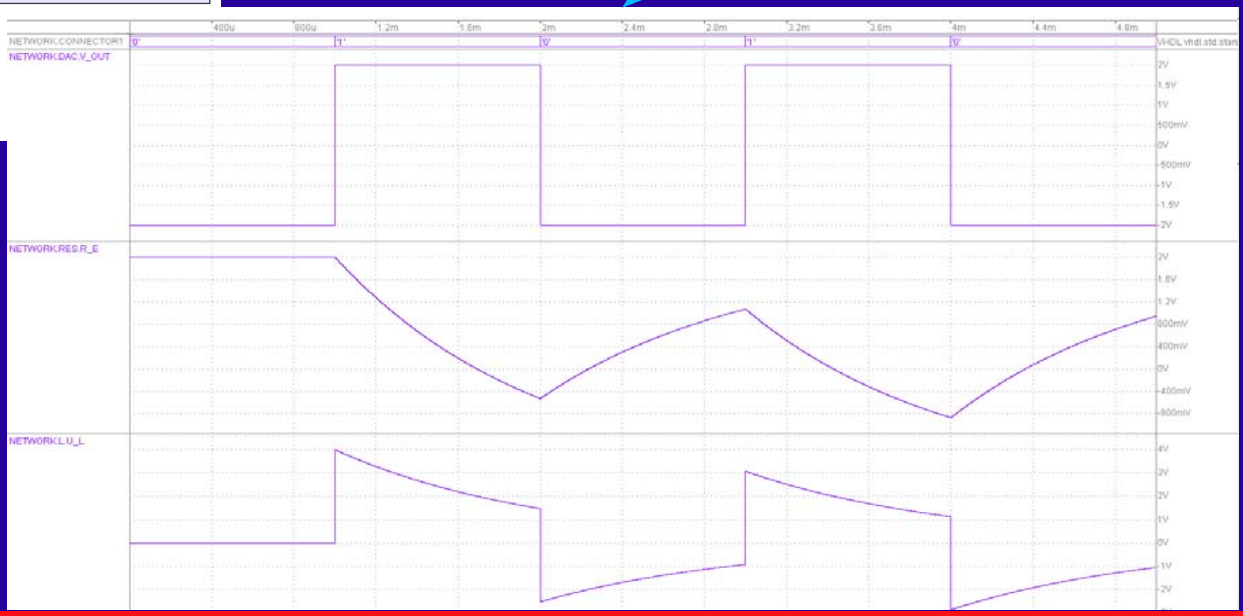
Simulate your SysML model!



The SysML model

A simulation trace



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Top reasons to virtual-prototype your model

- Keep documentation and model up-to-date
- Enable early testing of hypotheses and feasibility
- Enable to verify hardware and software at the same time (hardware in the loop)

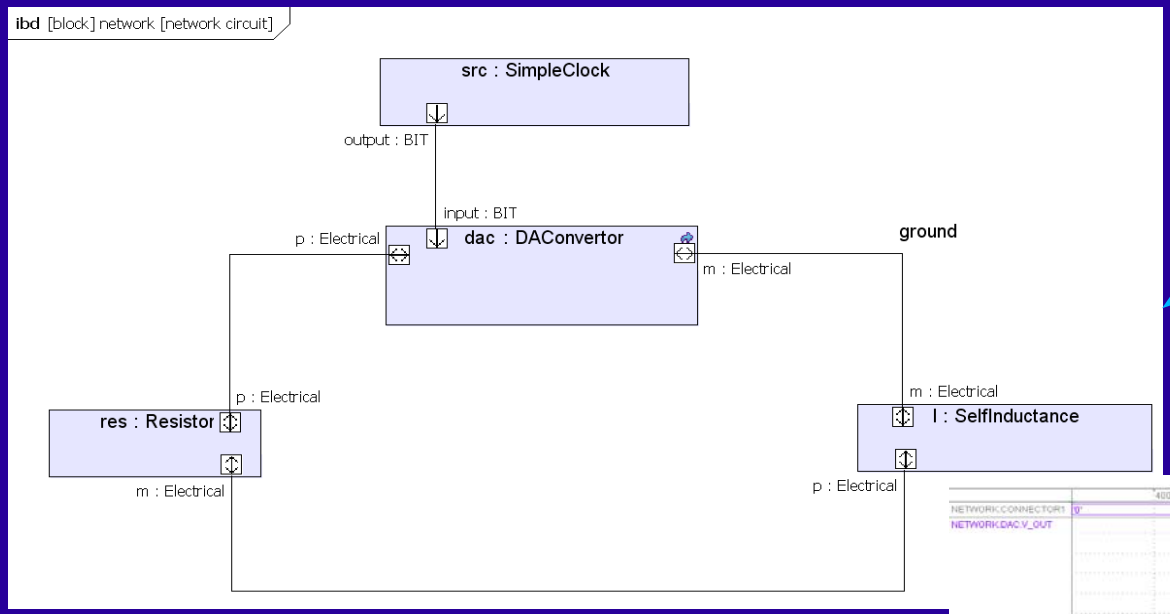
➔ Cut prototype cost

➔ Shorten time-to-market

Why SysML?

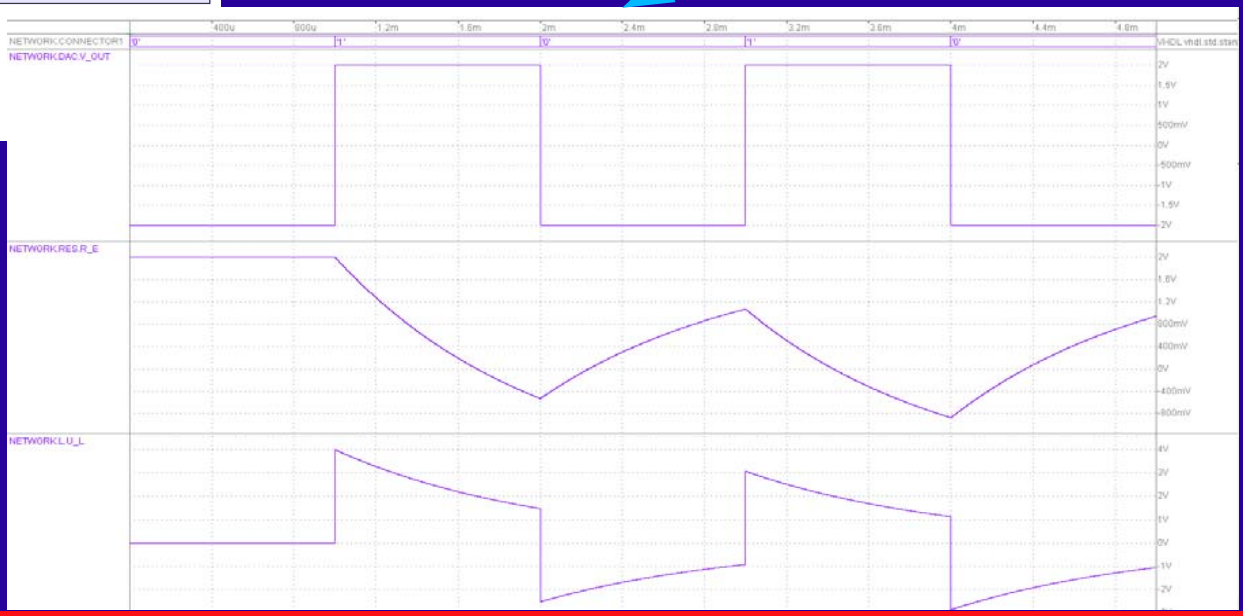
- “Lingua franca” between managers and engineers from different background
- Capture all important facets of your product
- Tools independent
- Standardized by OMG
- Technology independent
- Powerful extensible modelling language

How it works



The SysML model

Simulation trace



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Vhdl-Ams

Vhdl-Ams
simulator

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Why Vhdl-Ams?

- Vendor independent: IEEE Standard (1076.1)
- Multi-domain: continuous and discrete
- Many tools available

- Plan for Modelica and more

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SysML-Companion at work

The following slides illustrate the process on a simple circuit that mixes electronic and logic.

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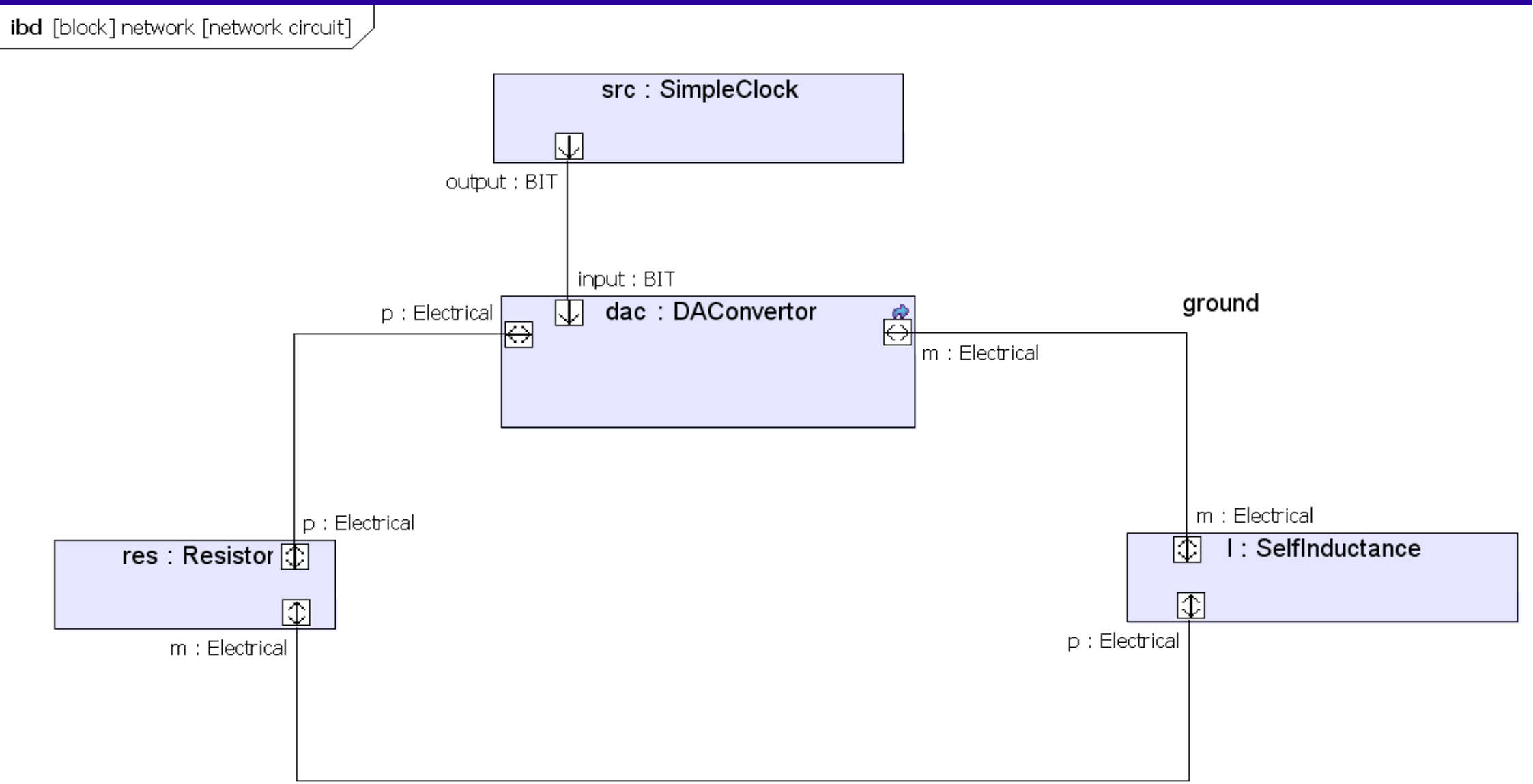
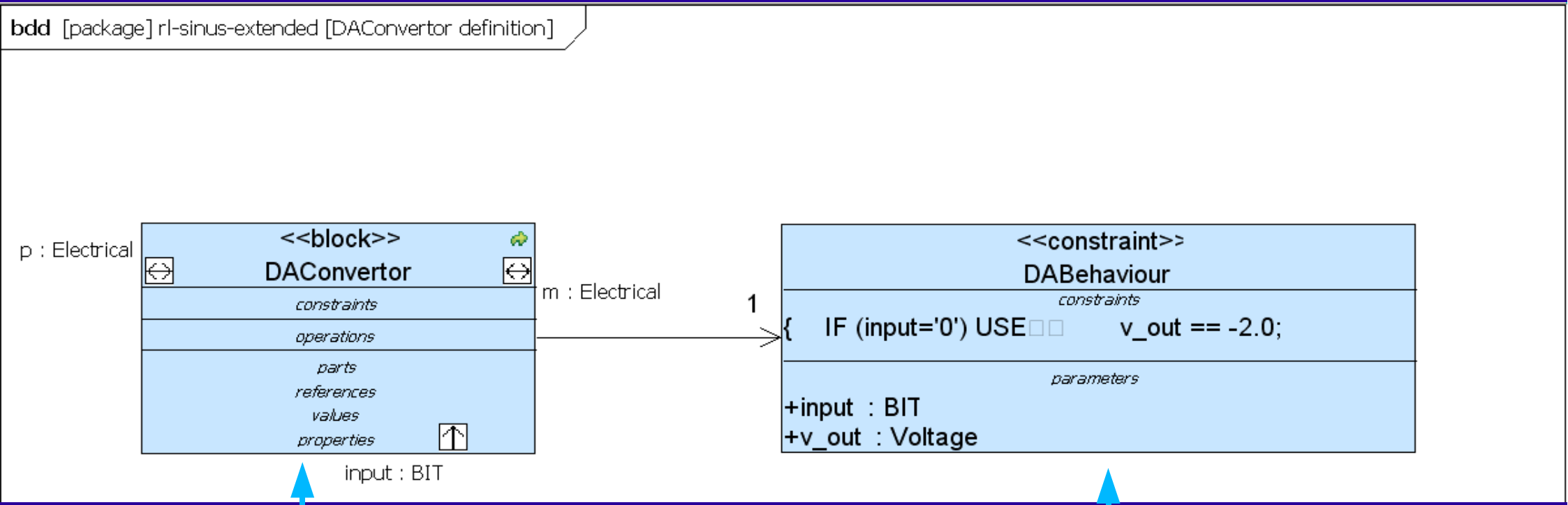
Description of a test circuit



Definition of the digital-analogic converter



Description of the “real” thing

The behaviour of the DAConvertor

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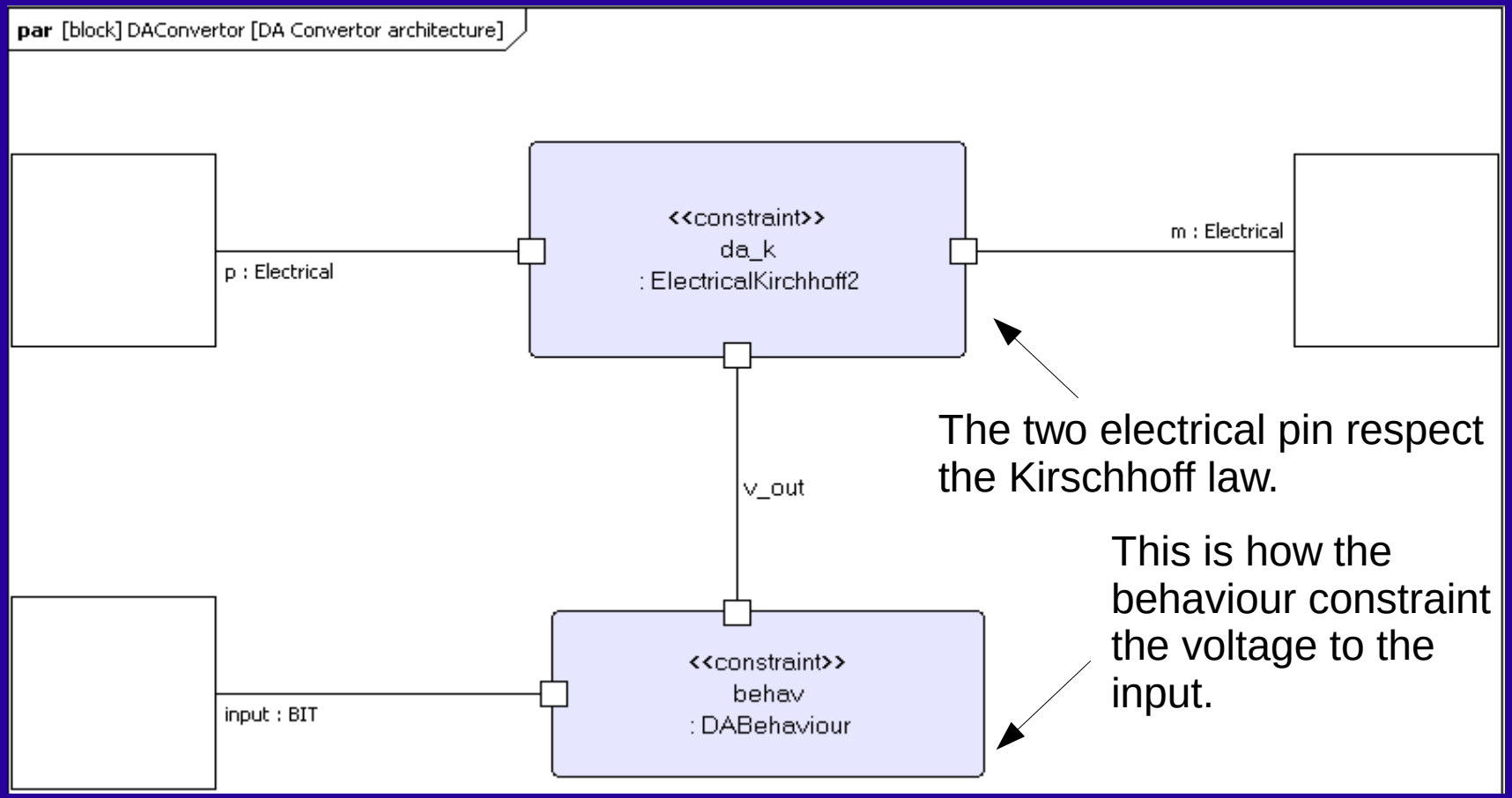
Parametric diagram describes the input/output relation



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Vhdl-Ams conversion

```
---------- ENTITY DECLARATION DAConvertor ----------
ENTITY DAConvertor IS

    PORT(TERMINAL p : Electrical;
      TERMINAL m : Electrical;
      SIGNAL input : IN BIT);
END ENTITY DAConvertor;

---------- ARCHITECTURE DECLARATION behav ----------
ARCHITECTURE behav OF DAConvertor IS

    QUANTITY v_out ACROSS i_out THROUGH p TO m;
BEGIN
    IF (input='0') USE
       v_out == -2.0;
    ELSE
       v_out == 2.0;
    END USE;
    BREAK ON input;
END ARCHITECTURE behav;
```

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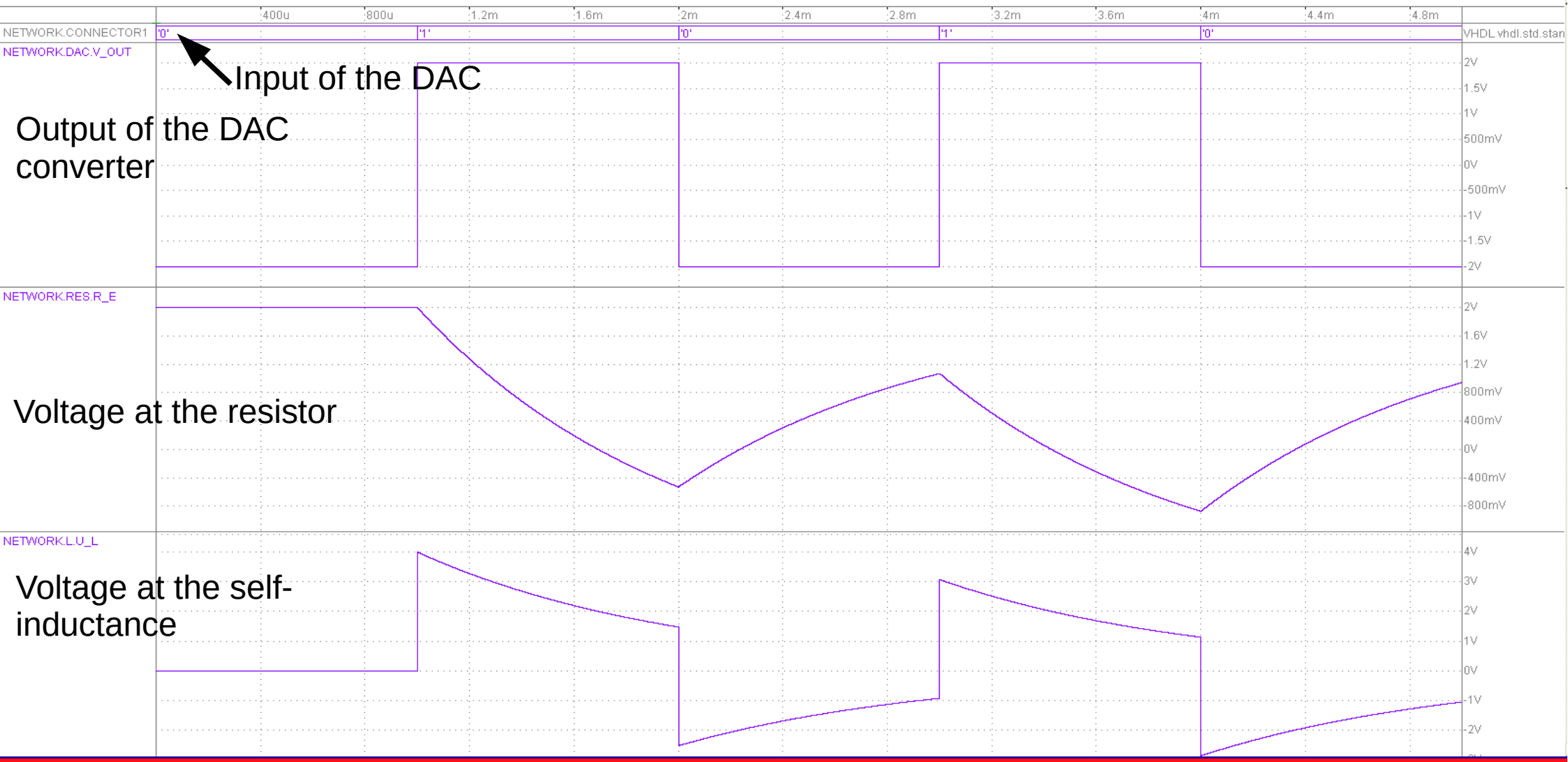
Simulation trace of the circuit



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