Strategies for End-to-End Timing Guarantees in a Centralized Software Defined Vehicle Architecture Combining CAN With TSN Backbone

SDV: Major Stakes

Def.

A New Software-Defined Architecture

Objective

Improve Cars Along Their Lifecycle

Connect Users To Ecosystems

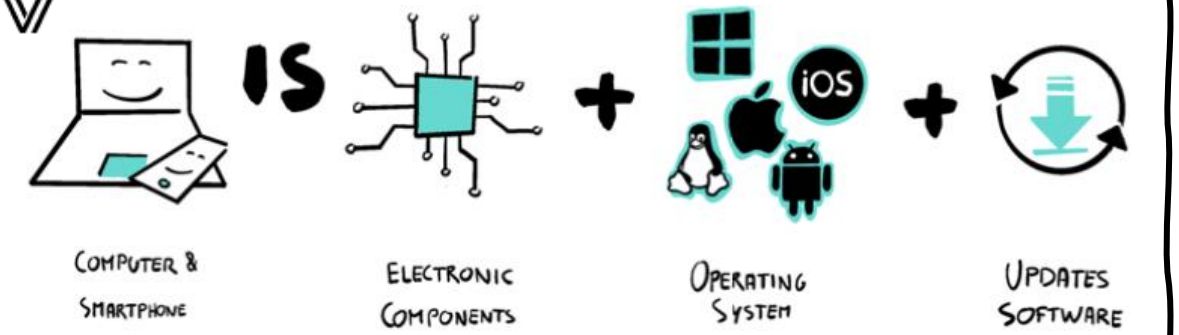
New Business Models

Report

Invest. In Autonomous Driving: +500B $

Invest. In Connected Autonomous Shared Electric

SDV



SDV = The same thing but **more** complex

Automotive Ethernet

Enabler of central EE/architecture & SDV

SW & HW decoupling with SOA communications

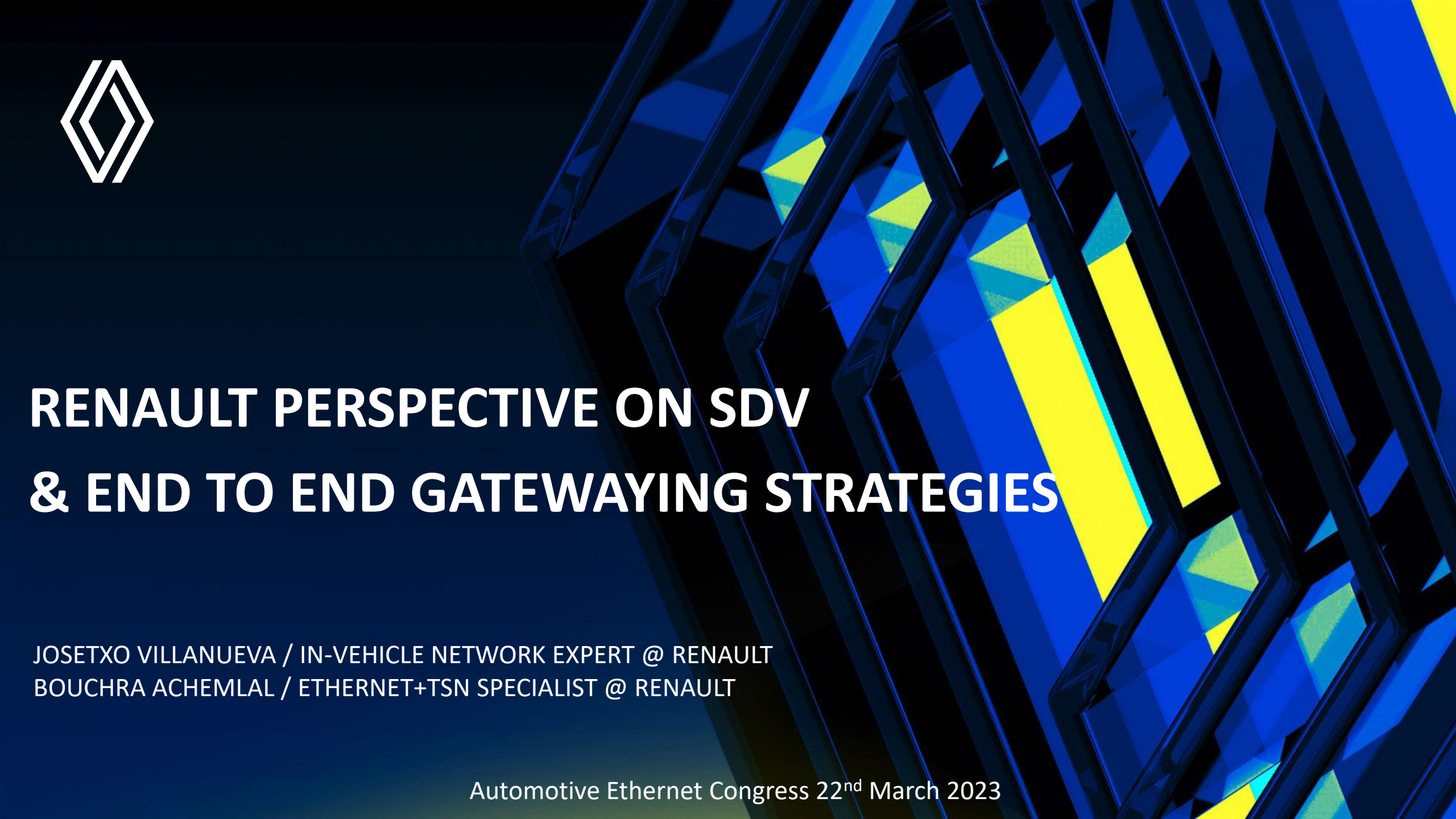
Challenges

- Meet E2E timings in SDV upgradable architecture
- Scalable gatewaying strategies
- E2E & TSN backbone configuration

Cooperation: Time experts, Tier-1, OEM

Agenda

- Renault Perspective on SDV & end to end gatewaying strategies
- RTaW Network Design and Validation Tools
- Bosch plugins in simulation for enhanced optimization
- Takeaways & Future Work

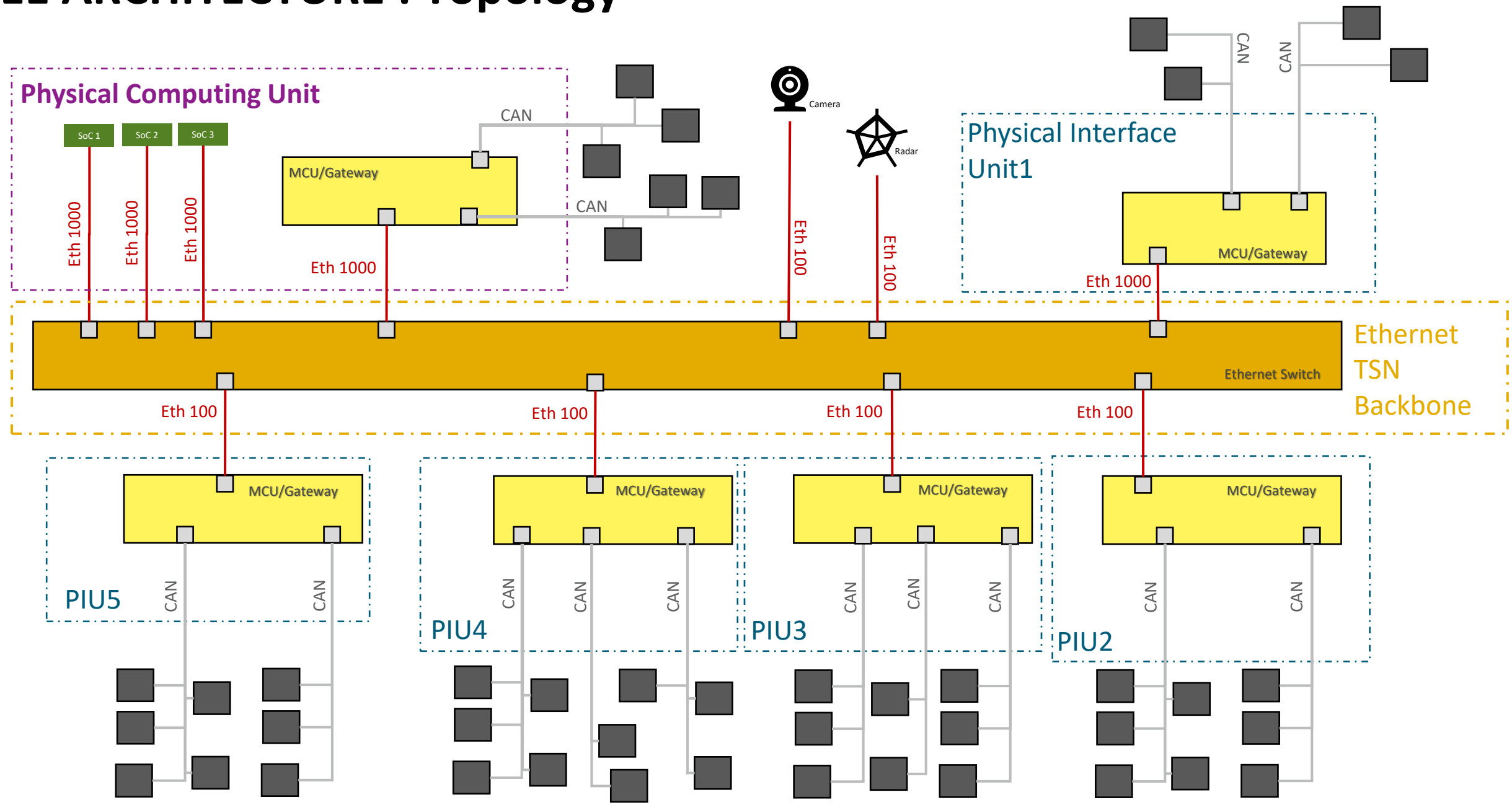


RENAULT PERSPECTIVE ON SDV & END TO END GATEWAYING STRATEGIES

JOSETXO VILLANUEVA / IN-VEHICLE NETWORK EXPERT @ RENAULT
BOUCHRA ACHEMLAL / ETHERNET+TSN SPECIALIST @ RENAULT

Automotive Ethernet Congress 22nd March 2023

EE ARCHITECTURE : Topology



EE Architecture : Constraints & Strategies

Mixed critical traffic

- **Command & Control** (Steering, Safety, Time-Constrained)
- **Sensor & Video Traffic** (Bursty data, ADAS, data fusion)
- **Audio streams** (Time sensitive, QoS, AR)
- **Diagnosis & Best Effort**
- **SDV Scalable Traffic (Future Features, OTA)**

Constraints

Switch
Buffer depth = f(BW, #ports, TSN config)

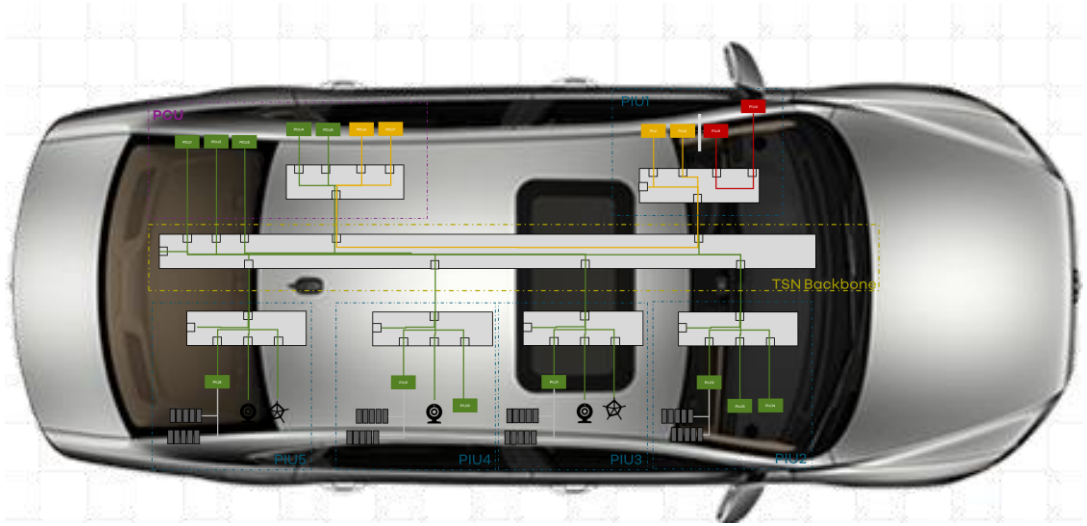
Gateways
Buffer depth=f(CPU load, Latency)

Avoid Packet Loss (Monitoring buffer usage)

Strategy

→ Control the CAN<->Ethernet Gatewaying

→ Deploy an appropriate TSN configuration



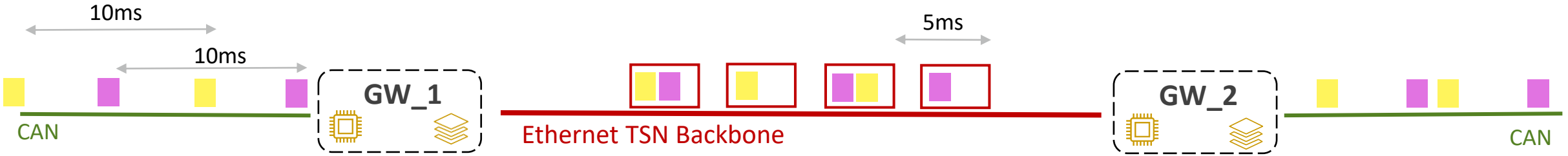
E2E CAN<->Ethernet Gatewaying Strategies

Command & Control traffic

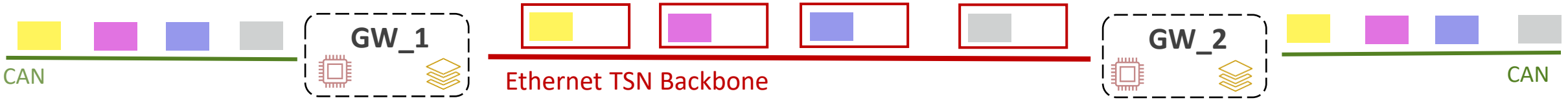
Buffer Depth

CPU Load

1. **Snapshot Strategy (PDU ½ period packing) ➔ Was simulated in a previous study (EIPATD 2019)**

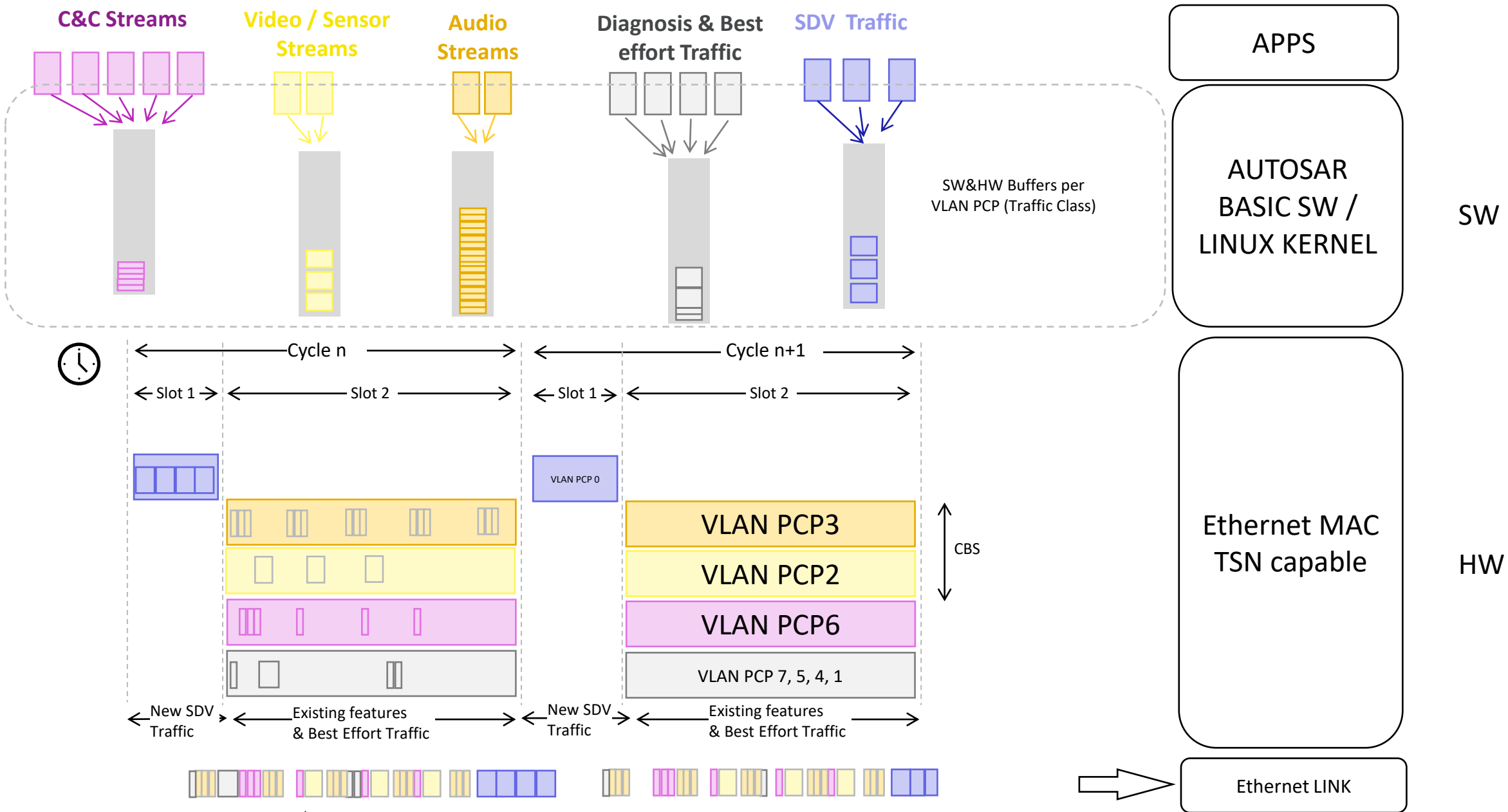


2. **1:1 PDU Packing ➔ will be studied in the simulation** (AEC 2023)



3. **All to 1 Packing ➔ will be studied in the simulation**

TSN DEPLOYMENT Strategy



Network Design and Validation Tools

Jörn Migge, CTO
RealTime-at-Work

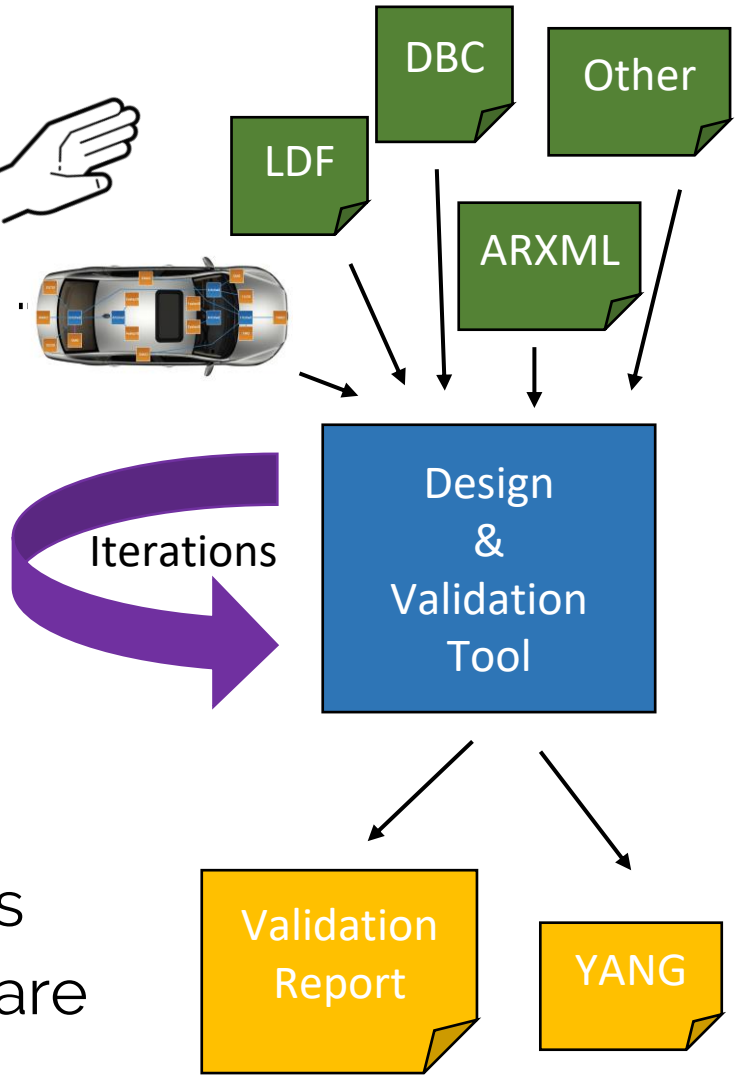
Automotive Ethernet Congress 22nd March 2023

Working with the tool

Input: which information is needed?
- Topology: link speeds, switching delays, connections
- Frames, PDUs, Services: periods, payloads, burst sizes, ..

Design & Validation
- Optimal configuration of TSN mechanism
- Validation of constraints through simulation & analysis

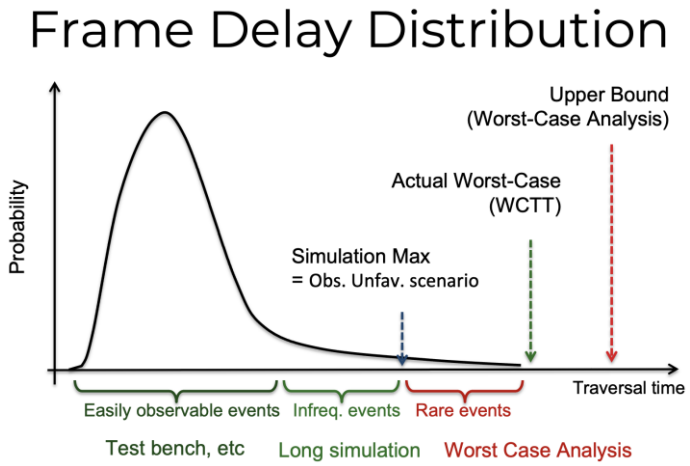
Output
- Validation report on latency and throughput constraints
- TSN scheduling parameters in YANG format for hardware

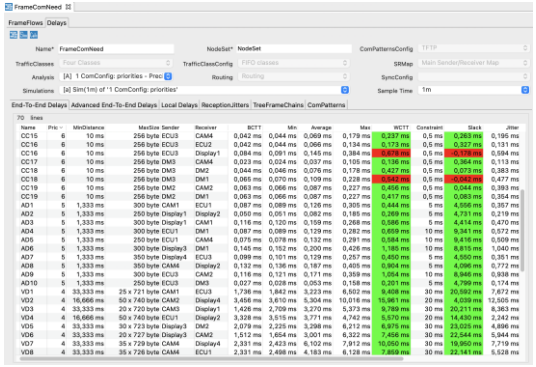


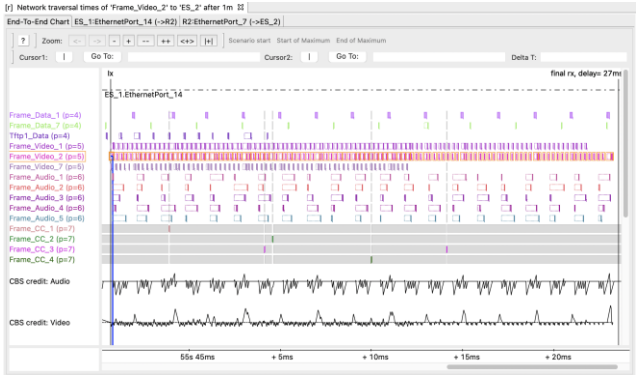
Roles of Worst-Case Analysis and Simulation

RTaW
RealTime-at-Work

- Worst-Case Analysis: computed upper bounds
  - Validation of (hard) latency and memory constraints
- Simulation: statistics
  - Validation of (soft) latency, memory and throughput constraints
  - Illustration through Gantt charts
  - Refined modelling through simulator plugins: gateways







Screenshots from RTaW-Pegase

CBS + CMI – video stream shaping

RTaW
RealTime-at-Work

Motivation

- Shaping of bursty traffic (generally) *reduces memory* requirements and *increases throughput* of lower priority traffic.

Difficulties

- Shaping means *delaying* the shaped frames, but their *latency constraints* must still be met!
- Not only shaping inside the network is useful but also at the *entrance of the network* (CMI, TSpec).

Solution

- CBS *configuration algorithm* based on *Worst-Case Analysis* to guarantee latency constraints.

TAS – for bandwidth partitioning

RTaW
RealTime-at-Work

Motivation

- Some *not well known or uncontrolled traffic* whose interference can be blocked through *bandwidth partitioning* with TAS.

Design choices

- *Size of the slots* for the two kinds of traffics => *period* of the gate control list.

Difficulties

- *Latency constraints*, not only of the shaped video stream must be met.
- *CBS* configuration must be adapted to the presence of *TAS* slots.

Solution

- CBS *configuration algorithm* based on *Worst-Case Analysis* able to cope with TAS + CBS.

Impact of CBS/CMI and TAS

	PCP	Frames	Nbr
900 us = 90%	6	SOMEIP / UDP	16
	5	CAN PDUs, SOMEIP / UDP	353 11
	4	SOMEIP / UDP	4
	3	Video	9
	2	Audio	1
	1	SOMEIP / TCP	416
100 us = 10%	0	SDV	87

CBS+CMI=250us

TAS: bandwidth partitioning

3 Configurations
(1) Only priorities
(2) CBS
(3) CBS+TAS

Delay Bounds(1)	TAS(3)	"Cost"
6.313 ms	8.436 ms	+ 33,6 %

Mem. Bounds(1)	CBS(2)	"Gain"	CBS+TAS(3)	"Gain"
1.079 MByte	0.080 MByte	- 92,5 %	0.165 MByte	- 84,6 %

Delay Max(1)	CBS(2)	"Gain"	CBS+TAS(3)	"Gain"
11.605 ms	6.300 ms	- 45,7 %	9.179 ms	- 20,1 %

Delay Max(1)	TAS(3)	"Gain"
14.265 ms	3.991 ms	- 72 %

Bound: computed by worst-case analysis
Max: observed in simulation

Plugins in simulation for enhanced optimization

Damon Martini
Robert Bosch GmbH
Communications Simulation Expert

Automotive Ethernet Congress 22nd March 2023

BOSCH

What is a plugin?

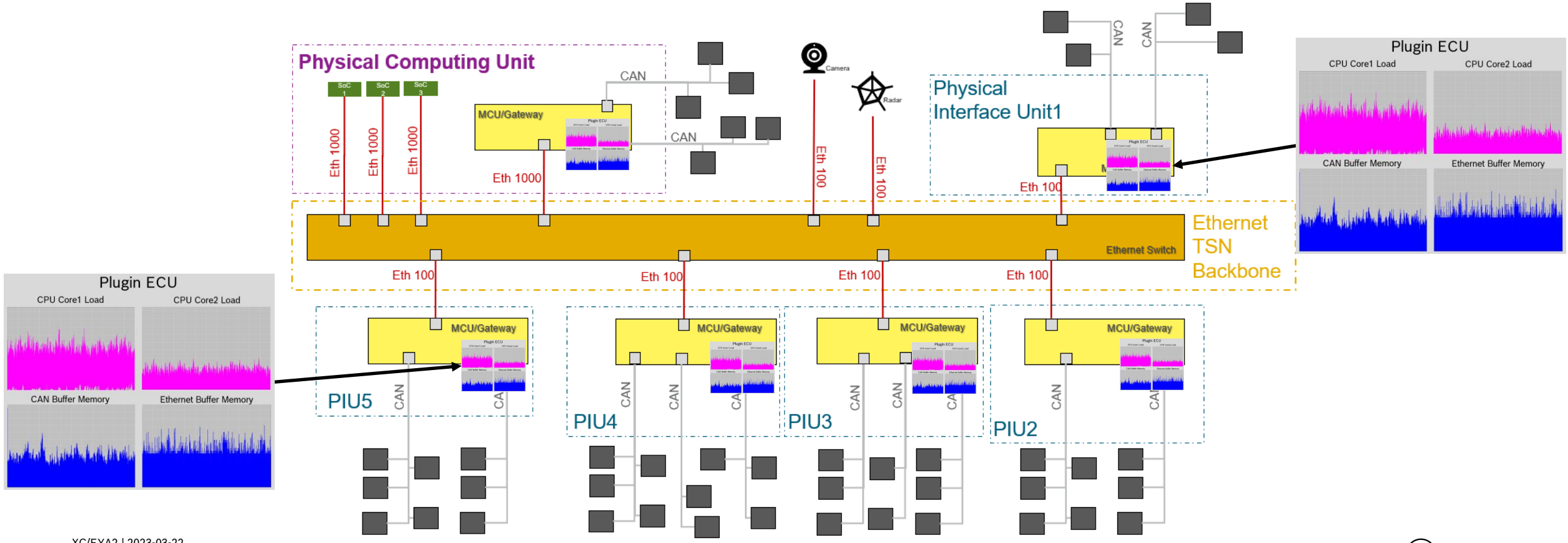
- Simply put a java model (or models) integrated into the RTaW Pegase simulation environment
- This plugin model can describe anything useful for network communications simulation:
  - Physical layer delays
  - Gateways (Autosar, other)
  - Ethernet switches

Why use plugins?

- ECU frame processing time is becoming a dominant factor in end to end latency compared to frame time on the wire
- Therefore it´s **VITAL** that these performance characteristics are included in the architecture modelling
- Also if we know the CPU load and input buffer memory we can better engineer the right microcontroller for the job

Plugins in the study context

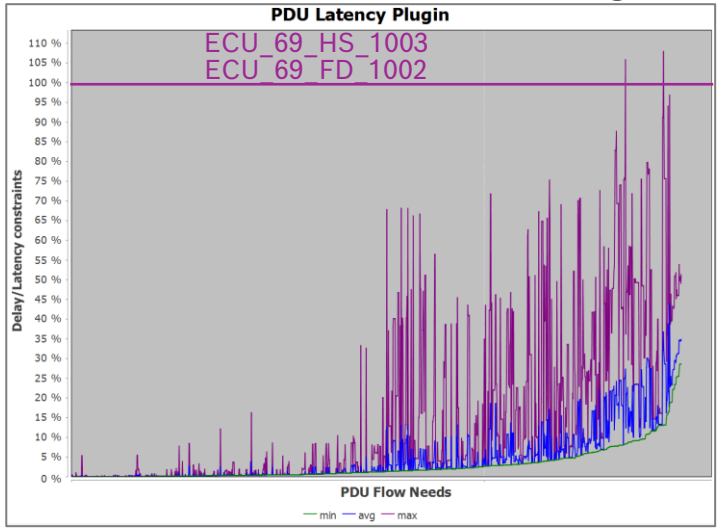
- Detailed modelling of Zone ECUs and Vehicle Computers
- Used for ECU optimization when packing/unpacking CAN PDUs transported over Ethernet

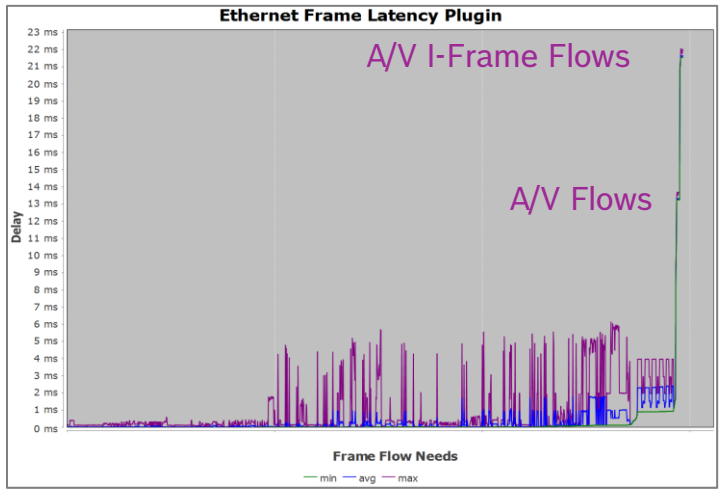


Results: PDU Latency & Ethernet Frame Latency

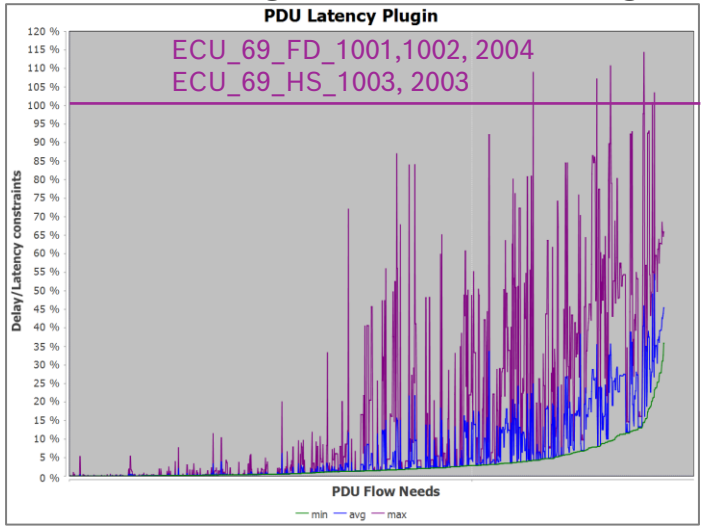
1:1 PDU Packing

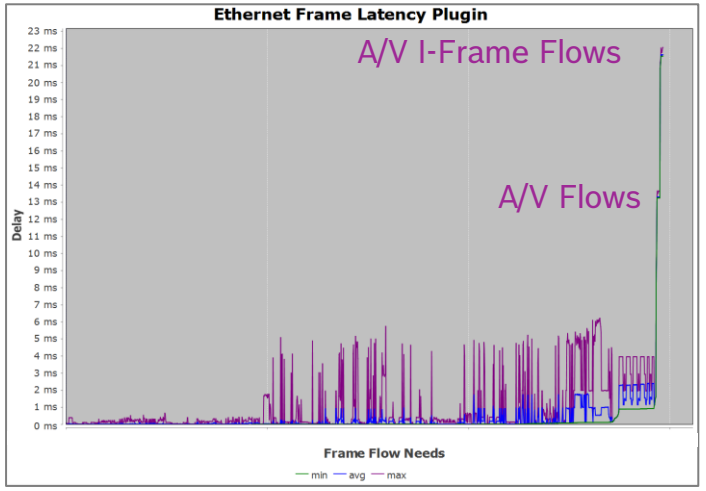
Interrupt Frame Processing





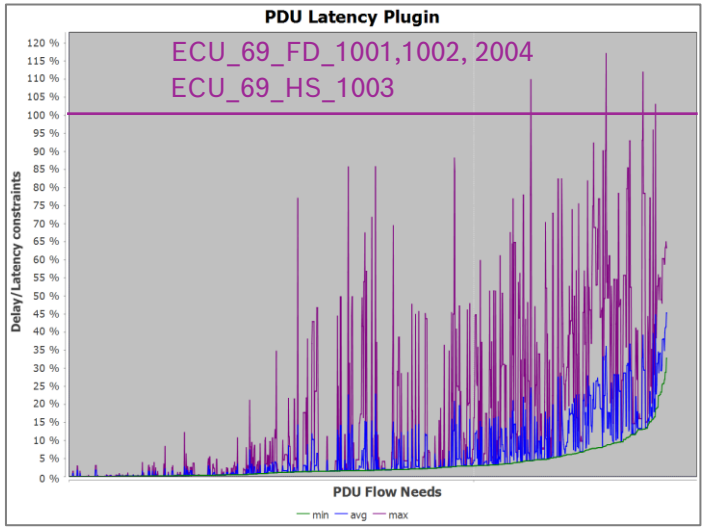
1ms Polling Frame Processing

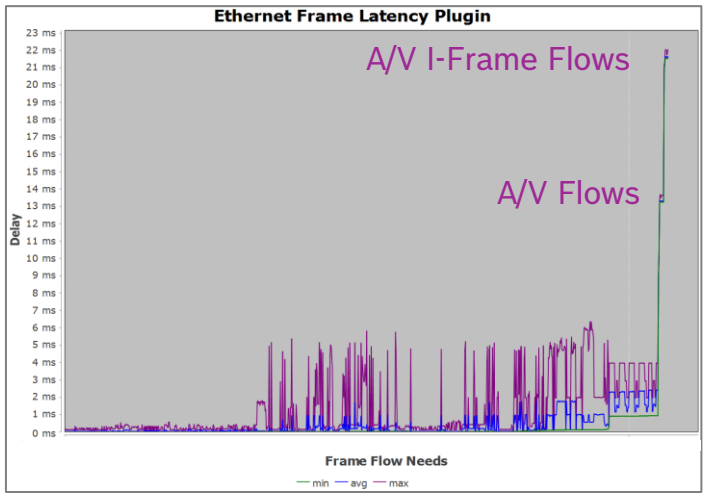




All to 1 Packing

1ms Broadcast



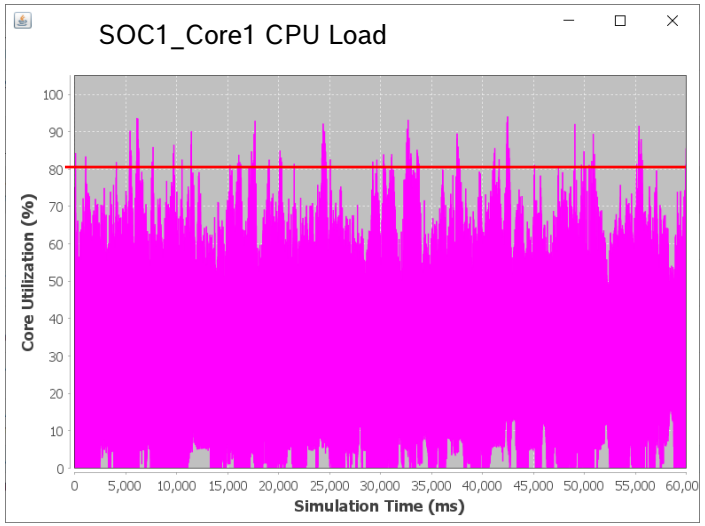


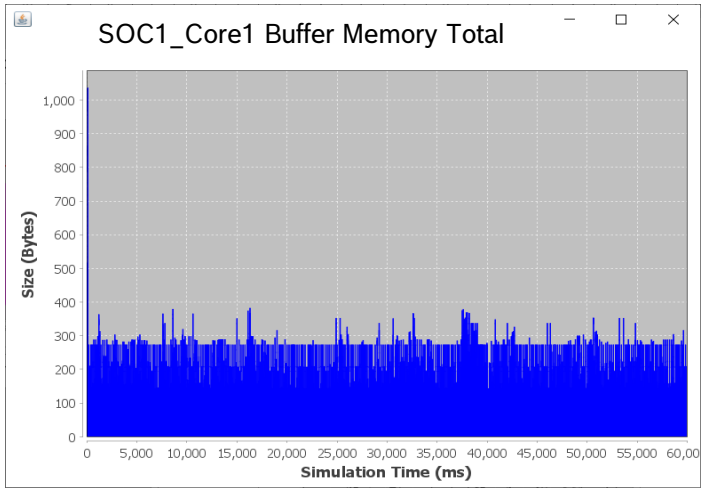
Results: CPU Load & Memory

Max allowed CPU load

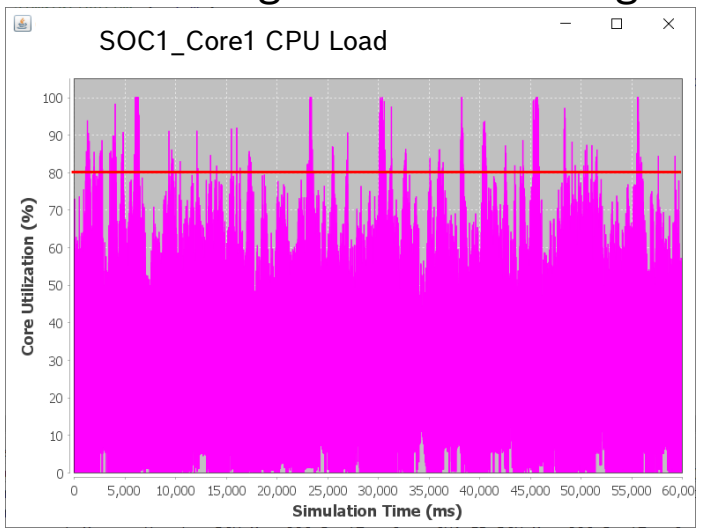
1:1 PDU Packing

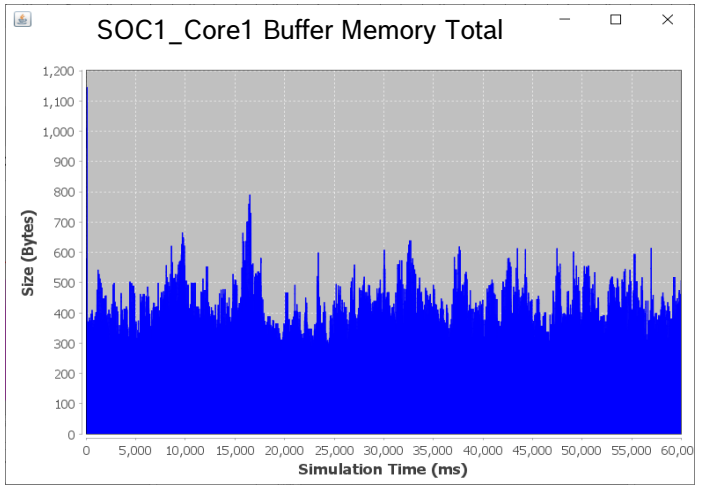
Interrupt Frame Processing





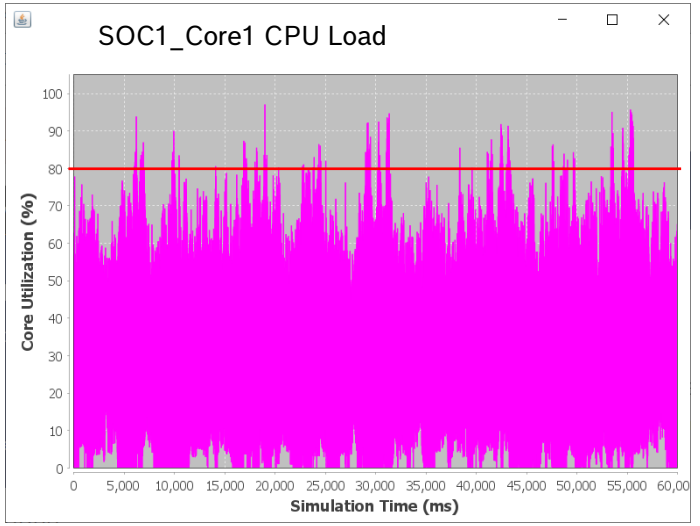
1ms Polling Frame Processing

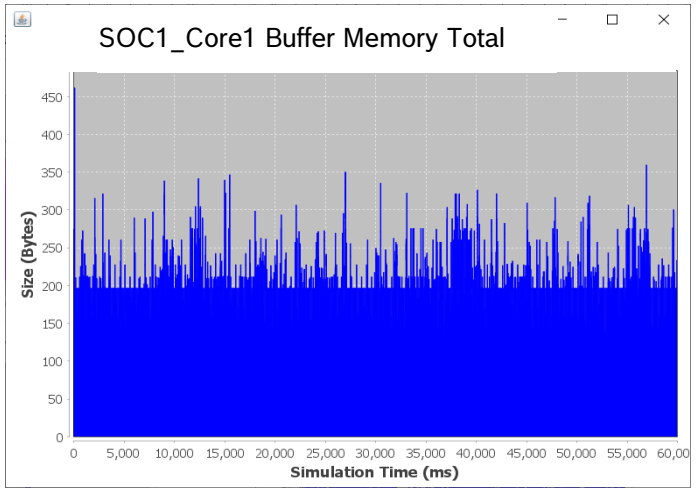




All to 1 Packing

1ms Broadcast





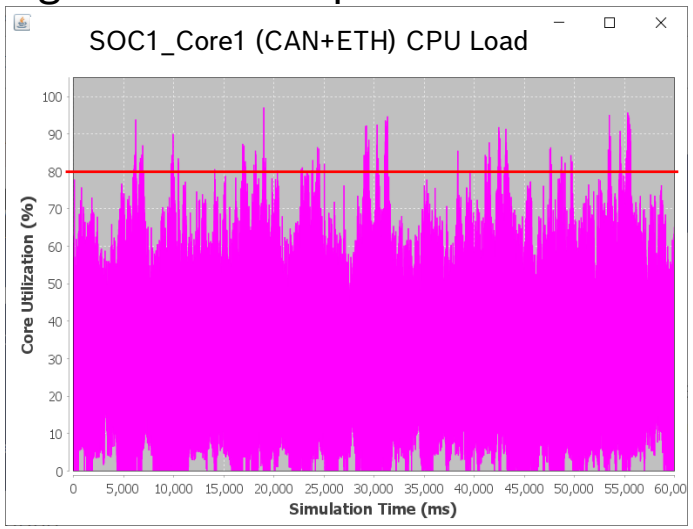
Results: CPU Load Single vs Dual Core

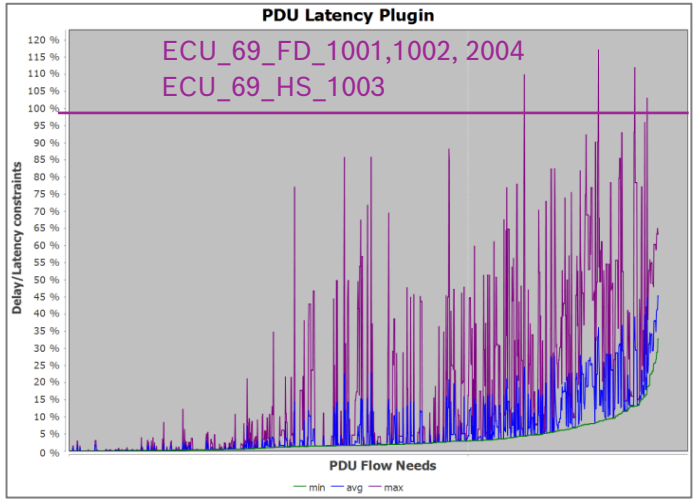
Max allowed CPU load

min avg max

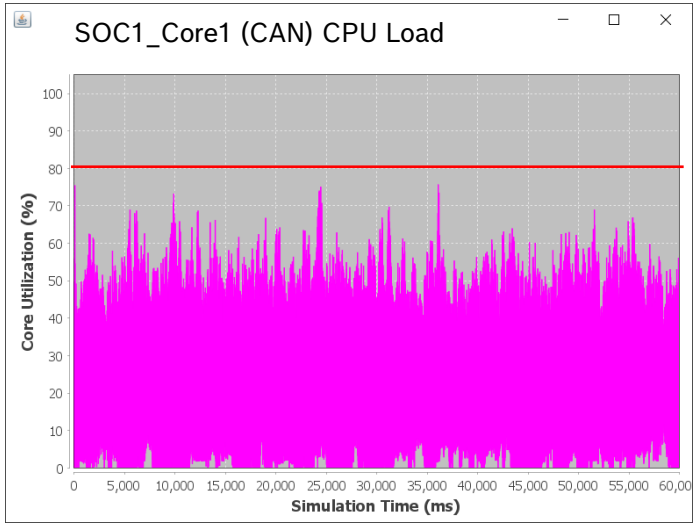
All to 1 Packing

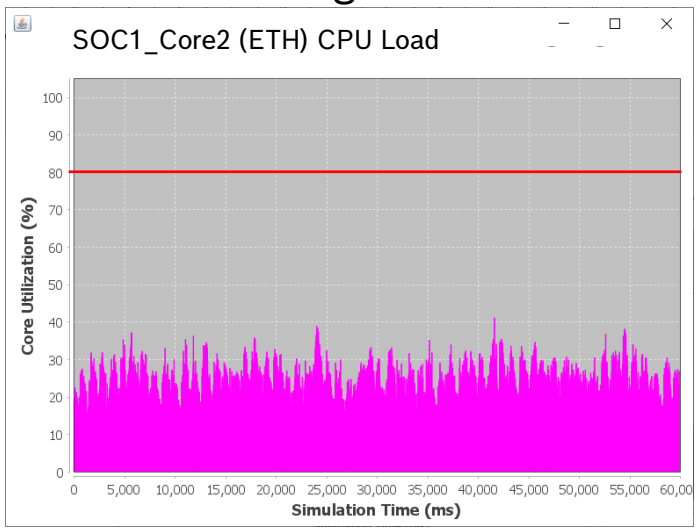
Single Core Interrupt Frame Processing

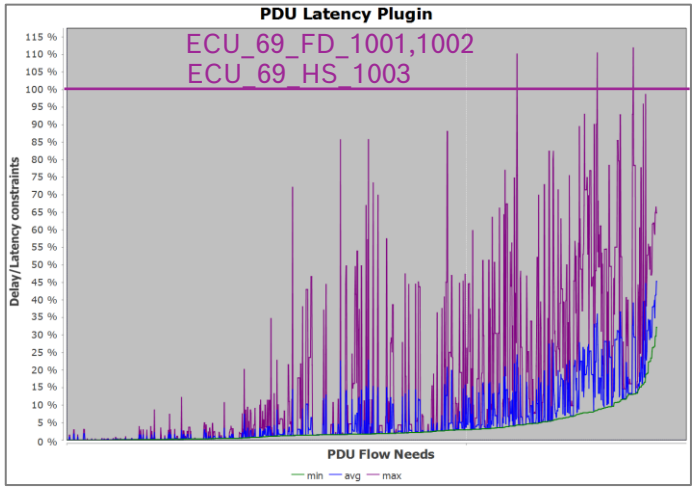




Dual Core Interrupt Frame Processing







Simulation Based Results

Optimization Step	KPI Analysis: PDU End to End Latency	KPI Analysis: Max Ethernet Link Loads (Top 3)	KPI Analysis: CPU Load	KPI Analysis: CPU Memory
1:1 Unicast (All processed by interrupt)	1476 from total of 1478 pass	47.96% 13.63% 12.50%	✗	Nº 2
1:1 Unicast (All processed by 1ms task)	1472 from total of 1478 pass	47.99% 13.63% 12.51%	✗	Nº 3
Many-1 Broadcast 1ms transmission (All processed by SingleCore interrupt)	1474 from total of 1478 pass	48.99% 21.58% 13.56%	✗	Nº 1
Many-1 Broadcast 1ms transmission (All processed by DualCore interrupt)	1475 from total of 1478 pass	48.91% 21.59% 13.56%	✓	Nº 1

Takeaways & Future Work

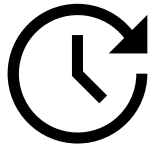
SDV Takeaways

CBS, Multicore gateways

TAS, Monocore gateways

- TSN strategy needs to be carefully considered to ensure the Ethernet switch resources don't become the bottleneck
  - Using TAS for scalability comes at a cost (2x buffer overconsumption)
  - CBS is effective in reducing Ethernet port memory usage and lower priority traffic latency
- To meet deadlines, CAN2ETH gatewaying latency needs to be < 1ms
  - Gatewaying strategy simulated doesn't impact link load or PDU latency – Services/Audio/Video are the main contributors
  - Putting CAN/Ethernet frame processing tasks on different cores achieves CPU load requirement

Future Work



Testbeds vs simulations
Qcr, PLCA, Multigig
GTW optimizations

- Correlating Ethernet switch buffer values and latency values from simulation with real implementation
- Exploring possible Ethernet backbone upgrades to ensure future scalability (eg: 10BASE-T1S, multi-Gb links)
- Simulating other scheduling mechanisms (eg: Qcr, PLCA)
- Gateway plugin optimization modeling
  - CPU loads via communication interface-CPU core mapping
  - use of Complex Device Drivers, hardware acceleration, IEEE 1722 Transport Protocol

Thank you

Questions?

Josetxo VILLANUEVA
In-vehicle Network expert
JOSE.VILLANUEVA@RENAULT.COM

Bouchra ACHEMLAL
Ethernet/TSN Specialist
BOUCHRA.ACHEMLAL@RENAULT.COM

BOSCH

Damon Martini

XC/EYA2
Cross-Domain Computing Solutions

damon.martini2@de.bosch.com

Contact: jorn.migge@realtimeatwork.com
C.T.O. RTaW